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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,607	04/14/2004	Albert Birner	0928.0052C	5077

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,607	BIRNER ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,9,11,14 and 16-26* is/are rejected.

7)☒ Claim(s) *6,7,10,12,13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/14/04; 06/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/823,607. Currently, claims 1-26 are pending.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the roughening step recited in claims 1, 16, and 21 must be shown or the feature canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 16-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "the silicon dioxide layer " lacks antecedent basis (claim 21, lines 14-15).

Claims 16 and 21 recite a step for exposing the silicon surface region/portion of the lower portion of the trench and a step for roughening the surface of the curved silicon surface region in the lower portion of the trench (claim 16, lines 10-13 and claim 21, lines 14-17). The relationship between the exposed silicon surface region/portion and the roughened surface is not clear. Since the roughening step is a critical element of the invention, the claims 16 and 21 should clearly recite that the exposed silicon surface region in the lower portion of the trench is that portion of the trench that is roughened. One suggestion would be to replace the phrase "roughening the surface of the curved silicon surface region" in both claims 16 and 21 be replaced with "roughening the exposed silicon surface region."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 8, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al (US 6,025,225) in view of Geusic et al. (US 5,981,350).

The Forbes et al. patent (Forbes) discloses a method for forming a trench capacitor (fig. 6 and accompanying text). The method comprises: providing a semiconductor substrate 616, the semiconductor substrate having at least one silicon surface region 620 having a curved surface (fig. 6 and col. 6, lines 50-55); roughening the silicon surface region to produce a layer of porous silicon, wherein roughening includes forming pores (fig. 6 and col. 6, lines 50-55); and forming a capacitor dielectric 622 on the roughened curved silicon surface region (fig. 6 and col. 6, lines 55-57)[1], wherein the depth of the roughened surface underlying the capacitor dielectric ends at a depth that is greater than the depth of the pores (fig. 6).

[1] See also col. 5, lines 59 - col. 6, line 8 and col. 6, lines 30-38.

In one disclosed embodiment, roughening of the silicon surface region includes etching the surface region, wherein the etching is performed in a solution containing phosphoric acid (col. 5, lines 59-65).

In another disclosed embodiment, roughening of the silicon surface region includes electrochemically etching the surface region, wherein the electrochemical etching process uses a 6% aqueous solution of hydrofluoric acid (col. 5, line 66 - col. 6, line 8).

As fig. 6 shows, the capacitor dielectric 622 has a thickness larger than the pore depth of the pores.

Forbes does not teach that the capacitor dielectric 622 is formed by thermally oxidizing the roughened silicon surface.

The Geusic et al. patent (Geusic) discloses a method for forming a trench capacitor (fig. 3 and col. 7, lines 9-36). As in Forbes, the method comprises: providing a semiconductor substrate 316, the semiconductor substrate having at least one silicon surface region 320 having a curved surface (fig. 3 and col. 7, lines 17-21); roughening the silicon surface region to produce a layer of porous silicon, wherein roughening includes forming pores (fig. 3 and col. 7, lines 20-23)[2]; and forming a capacitor dielectric 322 on the roughened curved silicon surface region (fig. 3 and col. 7, lines 22-25). Forbes further discloses using conventional oxidation to grow a capacitor dielectric (col. 7, lines 3-5). Thermal oxidation is a conventional oxidation method.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the capacitor dielectric 622 of Forbes by thermally oxidizing the roughened silicon surface region because thermally grown oxide is highly conformal and adheres well to silicon, thereby allowing the oxide to substantially completely fill the pores without forming voids.

While Forbes teaches that the smallest pore has a width of 2 nm (col. 6, lines 35-38), *Forbes does not teach that each pore has a width of less than 20 nm and a pore depth of less than 20 nm. Furthermore, Forbes does not teach that the size of each pore is less than 10 nm, or less than 5 nm.* However, Forbes does teach that the size and shape of the pores depends on the anodization parameters, and that by adjusting the parameters the diameter of the pores can be controlled (col. 6, lines 30-38).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form each pore having the sizes as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering an optimum value of a result effective variable involves only routine skill in the art (In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes in view of Geusic, as applied to claim1 above, and further in view of Nakamura et al. (US 5,739,565).

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[2] See also col. 6, lines 14-44.

As explained above, Forbes discloses roughening of the silicon surface region includes electrochemically etching the surface region, wherein the electrochemical etching process uses a 6% aqueous solution of hydrofluoric acid. *However, Forbes lacks anticipation of using a mixture of hydrofluoric acid and ethyl alcohol.*

The Nakamura et al. patent (Nakamura) discloses a method of forming porous silicon (figs. 1A-1E and accompanying text). The method comprises roughening a silicon surface region 1 to form pores 3 (col. 3, lines 23-25; col. 3, lines 31-38; and col. 3, lines 56-59). Roughening of the silicon surface region includes electrochemically etching the surface region, wherein the electrochemical etching process uses a mixture of 49% concentrated hydrofluoric acid and ethyl alcohol (col. 3, lines 39-47).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Forbes and Geusic by performing the electrochemical etching process using a mixture of hydrofluoric acid and alcohol, as taught by Nakamura, because the mixture provides an anodization current of sufficient magnitude to produce pores in the surface of the silicon surface region.

Allowable Subject Matter

6. Claims 6, 7, 10, 12, 13, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 16 and 21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. Claims 17-20 and 22-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The prior art of record does not anticipate, teach, or suggest a method of producing a storage trench capacitor for a memory cell having an isolation collar substantially as recited in claims 16 and 21, wherein the method comprises: exposing the silicon surface region of the lower portion of the trench, and roughening the surface of the silicon surface region to produce a layer of porous silicon.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
02 October 2005